



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,033	01/28/2000	Nobuyuki Yoshii	32178.157339	1679
26694	7590	10/27/2003	EXAMINER	
VENABLE, BAETJER, HOWARD AND CIVILETTI, LLP			SORRELL, ERON J	
P.O. BOX 34385			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20043-9998			2182	13

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/493,033	YOSHII, NOBUYUKI	
Examiner	Eron J Sorrell	Art Unit	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 7/30/03.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,2 and 8 is/are rejected.

7) Claim(s) 3-7 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 28 January 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>9 and 12</u> .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. The information disclosure statement (IDS) submitted on 1/28/00 has now been considered because applicant has re-submitted the foreign language references on 7/30/03 that were originally not present at the time of the initial examination. The IDS filed 7/2/03 has also been considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,2, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motomura (U.S. Patent No. 6,338,108) in view of Mesnik (U.S. Patent No. 3,748,651).

4. Referring to claim 1 and 8, Motomura teaches a packet communication apparatus for processing consecutive packets, the apparatus comprising:

a DRAM storage circuit (see item labeled 1 in figure 9A);

a first processing circuit which accesses the storage circuit for executing first processing with respect to data obtained from each of the packet (see item labeled 9 in figure 9A and lines 43-61 of column 23);

Motomura fails to teach a second processing circuit which accesses the storage circuit for executing second processing with respect to data stored in the storage circuit and an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of the packets, the allocation circuit allocating a first time period of the packet processing circuit for accessing the storage circuit and a second time period of the packet processing time to the second processing circuit for accessing the storage circuit, the first time period and the second time period being prevented from overlapping with each other.

Mesnik teaches an apparatus with first and second processing circuits connected to a storage device (see items labeled 20 and 26 in figure 5). Mesnik further teaches means for allocating a first time period of a packet processing time to the first processing circuit and a second period of a packet processing time to the second processing circuit for accessing the storage circuit, the first time period and the second time period being prevented from overlapping (see lines 51-62 of

Art Unit: 2182

column 1; Note Mesnik teaches the read and write cycle is lengthened to allow for the refresh to occur at the end of the read or write. Since the refresh happens at the end of the cycle there is no overlap).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Motomura with the teachings of Mesnik such that it comprises a second processing circuit which accesses the storage circuit for executing second processing with respect to data stored in the storage circuit and an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of the packets, the allocation circuit allocating a first time period of the packet processing circuit for accessing the storage circuit and a second time period of the packet processing time to the second processing circuit for accessing the storage circuit, the first time period and the second time period being prevented from overlapping with each other. One of ordinary skill in the art would have been motivated to make such modification in order to relieve the first circuit of having to request a refresh via an external command.

Art Unit: 2182

5. Referring to claim 2, Motomura teaches the storage device is a DRAM (see item labeled 15 in figure 8) and Mesnik teaches the second circuit refreshes the DRAM during the second time period (see Mesnik, lines 51-62 of column 1).

Allowable Subject Matter

6. Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J Sorrell whose telephone number is 703 305-7800. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703 308-3301. The fax phone number for the

Art Unit: 2182

organization where this application or proceeding is assigned is
(703) 872-9306.

Any inquiry of a general nature or relating to the status
of this application or proceeding should be directed to the
receptionist whose telephone number is 703 305-3900.

EJS
October 15, 2003



JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100